WHAT IS CLAIMED IS:

1. A control loop circuit for optimizing a power supply output under varying load conditions, the power supply having a main loop amplifier and an output stage to generate the output, the control loop circuit including:

a static control path coupled to the output and having an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output and a sensed output; and

a dynamic control path coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the dynamic control path having an output coupled to the main loop amplifier output.

2. A control loop circuit according to claim 1 wherein the dynamic control path includes:

input conversion circuitry for converting the error signal into a digital signal,

a digital-signal-processor coupled to the conversion circuitry;

a look-up table for storing optimal compensation signal responses to detected error signals, the DSP operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and

output conversion circuitry for feeding the optimal signal to the main loop amplifier output.

3. A control loop circuit according to claim 2 wherein:

the look-up table comprises a RAM memory.

4. A control loop circuit according to claim 1 wherein the dynamic control path is disposed in parallel with the static control path.

5. A control loop circuit according to claim 1 wherein:

the dynamic control path is selectively activated when the error signal is greater than a predetermined threshold.

6. A control loop circuit according to claim 2 wherein:

the output conversion circuitry comprises a digital-to-analog converter.

7. A control loop circuit according to claim 2 wherein:

the static control path includes respective source and sink signal paths; and

the output conversion circuitry comprises respective source and sink digital-to-analog converters coupled to the respective source and sink signal paths.

8. A control loop circuit for controlling the loaded output of a DUT power supply, the DUT power supply including a main loop amplifier and an output stage amplifier, the control system including:

means for statically generating an error signal and coupled between the input and output of the power supply; and

a dynamic control loop including a digital-signal-processor, the dynamic control loop disposed in parallel with the static control loop, the dynamic control loop selectively cooperating with the static control loop to optimize the power supply output in response to varying output loads.

9. A control loop circuit according to claim 8 wherein:

the means for statically generating an error signal comprises a static control path including an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier.

10. A power supply system including:

a main loop amplifier circuit;

an output stage disposed in cascade with the main loop amplifier circuit; and

a control loop circuit the control loop circuit including

a static control path coupled to the output and having an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output and a sensed output; and

a dynamic control path coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the dynamic control path having an output coupled to the main loop amplifier output.

11. A control loop circuit according to claim 10 wherein the dynamic control path includes:

input conversion circuitry for converting the error signal into a digital signal,

a digital-signal-processor coupled to the conversion circuitry;

a look-up table for storing optimal compensation signal responses to detected error signals, the DSP operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and

output conversion circuitry for feeding the optimal signal to the main loop amplifier output.

12. A control loop circuit according to claim 11 wherein:

the look-up table comprises a RAM memory.

13. A control loop circuit according to claim 10 wherein the dynamic control path is disposed in parallel with the static control path.

14. A control loop circuit according to claim 10 wherein:

the dynamic control path is selectively activated when the error signal is greater than a predetermined threshold.

15. A control loop circuit according to claim 11 wherein:

the output conversion circuitry comprises a digital-to-analog converter.

16. A control loop circuit according to claim 11 wherein:

the static control path includes respective source and sink signal paths; and

the output conversion circuitry comprises respective source and sink digital-to-analog converters coupled to the respective source and sink signal paths.

17. A method of controlling the output of a DUT power supply, the method including the steps of:

generating a static error signal based on the difference between the desired power supply output and the actual power supply output;

producing a dynamic error signal in parallel with the static error signal; and

summing the static error signal and dynamic error signal to create an optimal compensation signal.

18. A method according to claim 17 wherein the producing step is dependent on the magnitude of the static error signal being above a pre-set threshold.

19. A method according to claim 17 wherein the producing step includes the steps of:

converting the static error signal into a digital signal;

analyzing the digital signal;

creating a dynamic error signal based on the analyzing step; and

converting the digital dynamic error signal to an analog dynamic error signal.